YO! - A Time-of-Arrival Receiver for Removal of Femtosecond Helicity-Correlated Beam Effects^{*}

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Abstract. The G0 parity violation experiment at Jefferson Lab is based on time-of-flight measurements, and is sensitive to timing effects between the two electron helicity states of the beam. Photon counters triggered by time-of-arrival at the target mandate that timing must be independent of delays associated with different orbits taken by the two helicity states. In addition, the standard 499 MHz beam structure is altered such that 1 of every 16 microbunches are filled, resulting in an arrival frequency of 31.1875 (31) MHz, and an average current of 40 μ A. Helicity correction involves identifying and tracking the 31 MHz subharmonic, applying a fast/fine phase correction, and finally producing a clean 31 MHz trigger and a 499 MHz clock train. These signals are phase-matched to the beam arrival at the target on the order of femtoseconds. The 10 kHz output bandwidth is sufficiently greater than the 30 Hz helicity flip settling time (500 μ s). This permits the system to correct each helicity bin for any orbit-induced timing inequalities. A sampling phase detection scheme is used in order to eliminate the unavoidable $2\pi/n$ phase shifts associated with frequency dividers. Conventional receiver architecture and DSP techniques are combined for maximum sensitivity, bandwidth, and flexibility. Results of bench tests, commissioning and production data will be presented.

INTRODUCTION

G0 is an experiment at Jefferson Lab designed to measure parity-violating asymmetries in elastic electron-nucleon scattering as a function of momentum transferred to the nucleon. This will provide better understanding of proton charge and magnetic structure by describing contributions from up, down and strange quarks [1].

At the heart of the experiment is JLAB's ability to deliver highly polarized ($\sim 75\%$) electrons, and to alternately “flip” the helicity from $+z$ to $-z$ at a 30 Hz rate using a pseudo-random code. It is possible that small helicity-correlated offsets associated with the launching time of the electron bunches could occur, on order of femtoseconds. This effect would produce a perceived asymmetry in the calculated time-of-flight of the particles from the target to the focal plane detectors.

The YO! Box produces two beam-derived signals, CLK and Y_0 , which are synchronized to the arrival of the electron bunches in experimental Hall C, rather than to the laser-pulse associated with the time of launch in the Injector. In addition to tracking any time-of-flight variations, it is mandatory that the receiver be unaffected

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by variations in beam intensity and position. Also, RF sampling was chosen as an alternative to prescaling in an effort to remove the inevitable $2\pi/n$ phase ambiguity associated with frequency dividing. This ambiguity would create arbitrary cycle slips, catastrophically confusing the triggering of the photon detectors. Tight phase control and monitoring are also required to prevent cycle slips from within the control system.

The G0 beam is a modified 499 MHz CEBAF bunch structure, whereby only every 16th bucket of 2 ps duration contains electrons, but with 16 times the intensity. This results in a 31 MHz sub-harmonic whose lower-limit level is nominally -95 dBm after redistributing the pulse-power energy and combining with the response from a standard stripline BPM designed for 1497 MHz operation. Although the S/N is too low for high precision timing, a filtered signal is easily derived for use as a sampling reference. Also available is energy from a resonant 1497 MHz BCM cavity, which is much greater (-20 dBm) and affords good S/N ratio for fine / fast tracking.

Timing is derived by phase-locking a stable 31.1875 MHz VCXO to the -95 dBm 31.1875 MHz sub-harmonic. The clean VCXO signal output is used to stroboscopically sample the 1497 MHz beam-derived signal with a Sampling Phase Detector (SPD), establishing a high resolution (ps) zero crossing with 10 kHz bandwidth. This phase correction is applied back to the 31 MHz VCXO signal, defining the time-of-arrival. Finally, the corrected VCXO signal is again used to sample a Master Oscillator-derived (MO) 499 MHz signal, applying the phase correction and aligning the 499 signal to create a CLK output. Figure 1 is an overview of the system.

FIGURE 1. Receiver system overview.

RECEIVER ARCHITECTURE

A hybrid analog / DSP architecture was selected primarily to piggy-back other development efforts at JLAB. Although the baseband FPGA-based DSP processor board was specifically designed for the YO! Receiver, it also resulted in a development tool for similar projects, and provided an ideal platform from which to develop the control algorithm. Due to the low noise figure requirement, combined with moderate output bandwidth, conventional RF front-ends were designed, but also included the use of Sampling Phase Detectors (SPD) for direct-conversion to baseband. Figure 2 is the block diagram of the entire receiver system.

In addition to bench testing sub-assemblies, extensive modeling using SystemView (Matlab) was performed in order to verify SPD operation, generate filter coefficients, and also check initial PID parameters for the control algorithm.

FIGURE 2. Receiver system block diagram

SAMPLING PHASE DETECTOR (SPD)

The fundamental advantage of the SPD, exploited by the YO! Receiver, is the ability to compare the phases of harmonically related signals, as opposed to conventional phase detectors which require identical frequency inputs. The concept of stroboscopically sampling a fast signal with an integral subharmonic has a rich and fascinating history [2]. References from as early as 1904 appear in literature [3], and were the basis for advancing vacuum tube technology to the point of observing microwave frequencies, resulting in affordable microwave instrumentation [4].

Although modern passive SPDs incorporating step-recovery diodes were initially investigated, they were found to be too lossy and fussy, and only moderate success was

achievable in trial runs [5]. Ultimately, the selected SPD was based on a circuit which first appeared in a General Electric Transistor Manual in 1964 [6]. NIST-based equivalent-time sampling circuits using comparators also provided promising results, but not at the intended operating microwave frequency [7,8]. A circuit using a PECL flip-flop and integrator was found which operates on the principle of balancing the Q and $\bar{Q}$ output durations by precisely holding the input at the logic decision threshold [9]. Feedback is used to balance the bias point at a metastable region, making the system highly sensitive to input perturbations. Input disturbances appear as pulse-width modulation on the Q-outputs, which are low-pass filtered and integrated, appearing as a voltage after the integrator. Since PECL operates well into the microwave region, its speed was adequate for 1497 MHz operation.

Since the sampling is synchronous, it possesses inherent noise immunity (much like a lock-in). In addition, the circuit is lossless, preserving the overall system noise figure [9].

A serious drawback to the single SPD is 2-quadrant operation, resulting in ambiguity between quadrants I/III and II/IV. This could either be resolved by dithering, or by using two SPDs in a quadrature configuration.

DSP BASEBAND PROCESSOR

Figure 3 illustrates the general functionality of the DSP Board. It consists of 4 analog-to-digital converter (ADC) stages, 4 digital-to-analog converter (DAC) stages, a FPGA, and multiple status and control inputs/outputs. The ADCs and DACs have a resolution of 16-bits and are updated at a rate of 150 kHz. Each ADC is preceded by an op-amp stage used for anti-alias filtering, scaling, and offsetting. The DAC outputs are also buffered with an op-amp stage used for scaling and filtering update-related noise.

FIGURE 3. FPGA-based DSP processor

The digitized Sampling Phase Detector (SPD) signals are sent to the FPGA where they are first passed through an IIR filter then a PID algorithm. The IIR filters have a 3 dB roll off of 500 Hz and are implemented using equation (1). The filter constants (a_1 , b_0 , and b_1) where derived using simulation software and scaled appropriately for this application. The variable n represents a discrete sample time, $x(n)$ is the signal input, and $y(n)$ is the filter output.

$$y(n) = a_1 * y(n-1) + b_0 * x(n) + b_1 * x(n-1) \quad (1)$$

The PID algorithm is accomplished with equations (2) and (3). The expression $e(n)$ is the filtered SPD error signal input, $S(n)$ is the integral term, and $u(n)$ is the PID output. The PID constants (K_P , K_I , and K_D) can be selected with jumpers, updated using an optical encoder knob, and displayed via status LEDs. Once the control loop has been tuned, the associated PID constants are hard coded into the FPGA.

$$u(n) = K_P * e(n) + K_I * S(n) + K_D * [e(n) - e(n-1)] \quad (2)$$

$$S(n) = \frac{S(n-1) + [e(n) + e(n-1)]}{2} \quad (3)$$

The control logic monitors the Received Signal Strength Indicators (RSSI) and the 31 MHz Phase Adjust in order to intelligently switch the 31 MHz input signal and establish lock. The RSSIs are used to determine if the signal levels are high enough to maintain lock. When the RSSIs become too low, the DSP Board freezes the IIR-PID-31 MHz Phase Adjust output chain and switches the chassis to an external 31 MHz reference. When the RSSIs return to an acceptable level, the chassis is switched back to the 31 MHz input. The IIR-PID-31 MHz Phase Adjust chain remains frozen for 50ms to permit the 31 MHz input signal to propagate through the chassis and into the

DSP board. This allows for seamless switching back-and-forth between the input signal and reference. If the chassis loses lock (the 31 MHz Phase Adjust rails) the DSP Board automatically resets the IIR-PID-31 MHz phase adjust chain in an effort to re-establish lock. The Phase Adjust outputs are limited to discourage multiple lock points and to ensure that the same lock point is found each time. The control logic also provides various status outputs to indicate the state of the chassis.

TESTS

Along with component and sub-assembly testing, system performance tests were required as a condition of customer certification. Of these, static bench tests were performed which measured such parameters as phase detector scaling, residual offset voltages, sensitivities to varying beam currents and positions, and slow signal tracking. Dynamic measurements included open and closed-loop responses, output BW, loop damping / settling time, and tangential sensitivity to 31 and 1497 MHz. Finally, beam-based tests were performed to provide the in-situ calibration data needed for accurate conversion from voltage data to engineering units.

Attempts to fully characterize the dynamic behavior of the YO! Receiver were performed using an HP 89410 Dynamic Signal Analyzer. The following stimulus-response tests were performed by modulating a pre-characterized voltage-variable phase shifter to induce a known phase delay, verifying frequency response of the PID in closed-loop, as well as to determine tangential sensitivity at a 30 Hz modulation frequency (ultimately reported in fs). Figure 4 shows the measured results of the final 499 MHz phase loop, confirming the well-behaved 10 kHz loop BW (100 μ s response time) for the entire system. Figure 5 demonstrates 10 dB S/N for a measurement of a 1ps equivalent delay. Subsequent tests using lower phase noise RF sources produced tangential sensitivities at the 10 fs level. All tests were performed with nominal 40 μ A simulated beam: $P_{31} = -80$ dBm, $P_{1497} = -20$ dBm, $S/N \geq 20$ dB.

FIGURE 4. Dynamic stimulus-response test plots of 499 MHz phase-loop control (a) and error signals (b), performed using HP89410 Dynamic Signal Analyzer.

FIGURE 5. Measurement of 1ps equivalent phase delay at 30 Hz modulation, demonstrating > 10 dB S/N.

After installation in the experimental hall, test plans were executed, which verified the sensitivity as well as the proper scaling of the time-of-flight measurements. Since the relationship between magnet current and resulting path length within the accelerator is reasonably well known, the easiest method was to wiggle a dogleg magnet in the accelerator arc, intentionally modulating the path length by ± 2 ps. Data was gathered using a PC104-type single-board computer serving EPICS, and producing real-time statistics and FFTs. Figure 6 displays the measured delay (in ps) vs. dogleg magnet flux (g-cm).

FIGURE 6. YO! Receiver output response of 499 MHz phase control signal vs. Dogleg magnet setting.

Although the G0 experiment was in-progress at the time of this writing, off-line data was analyzed at the 50% mark to verify proper operation. Of most interest were the immunities to current intensity fluctuations, as well as position. Figure 7 demonstrates both effects, resulting in certification of the receiver system by the G0 Collaboration [10].

FIGURE 7. Demonstration of immunities to beam intensity (a) and beam position for X (b) and Y (c). TDC bins each represent 35 ps.

OTHER APPLICATIONS

As is usually the case for new systems, measured data often describes an effect previously unmeasurable by existing hardware. The ability to measure pathlength at the end-station with high speed and resolution provides a feedback mechanism for energy locks, helicity control at the target, as well as corrections associated with seasonal machine growth. Finally, a multi-channel, multi-frequency vector voltmeter spinoff project is being produced for the purpose of Injector RF Phase monitoring, whereby an MO-derived 1497 MHz signal is used as a reference to quadrature SPDs, providing ps-level resolution with 1 Hz update rates.

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