Development of BPM Electronics at the JLAB FEL

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Abstract. A new version of BPM electronics based on the AD8362 RMS detector, which is a direct RF to DC converter, is under development at the JLAB FEL. Each of these new BPM electronics utilizes an embedded ColdFire Microprocessor for data processing and communication with the EPICS control system via TCP/IP. The ColdFire runs RTEMS, which is an open source real-time operating system. The JLAB FEL is a SRF Energy Recovery LINAC capable of running up to 10 mA CW beam with the micropulse up to 74.85 MHz. For diagnostic reasons and for the machine tune up, the micropulse frequency can be reduced to 1.17 MHz, which corresponds to about 160 μ A of beam current. It is required that the BPM system would be functional for all micropulse frequencies. By taking into account the headroom for the beam steering and current variations the dynamic range of the RF front end is required to be about 60 dB. A BPM resolution of at least 100 μ m is required, whereas better resolution is very desirable to make it possible for more accurate measurements of the electron beam optics. Some results of the RF front end development are presented as well as the first measurements made with an electron beam.

Keywords: BPM Electronics, ColdFire, AD8362

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INTRODUCTION

The BPM electronics that are under development are intended to be stand alone devices that do not require any outside system such as VME or CAMAC. These stand alone electronics are divided into two major sub-sections to achieve the desired functionality. The first section, the RF Front End, down converts the 1.497 GHz RF input to DC. Once the signal is in DC, it then propagates to the second sub-section, the digital portion of the electronics. The Digital section of the electronics is responsible for data processing as well as TCP/IP communication. The physical size of these electronics is a major design constraint in order to minimize cost. Several series of functionality tests and measurements were made for these electronics. With this data and the initial intent for these electronics to be prototypes, some modifications will be made before these are deployed throughout the FEL.

ELECTRONICS DEVELOPMENT

RF Front End

These electronics are being developed for use with the Strip Line BPM Cans. Measurements were made from existing BPMs within the FEL to determine the RF Front End bandwidth and signal intensity levels. The data shown in Fig. 1 shows the data taken from 100 μA to 1 mA and the extrapolated data from 10 μA to 10 mA. This illustrates that in order to meet the specifications for 1.17 MHz to 74.85 MHz the dynamic range of the front end should be about 60 dB.

FIGURE 1: Dynamic Range of FEL beam signal as a function of current

Once the bandwidth of the FEL was determined to be about 60 dB it was decided that the AD8362 RMS detector should be the center building block for the RF Front End, since its bandwidth too is also about 60 dB [1]. The conceptual design was to implement the AD8362 to down convert the 1.497 GHz to DC and then process the DC signals with an ADC and microprocessor. Figure 2 details a schematic of one channel of the developmental BPM electronics.

FIGURE 2: One Channel schematic of BPM Electronics

Digital Section

The intention for these electronics was for each set to have a dedicated on board processor. The processor implemented was the Arcturus uCdimmm version of the Motorola ColdFire 5282 [2]. The processor is implemented with RTEMS as the operating system and utilizes TCP/IP to directly communicate with the EPICS control system. Each of the processors are capable of being remote programmed and rebooted. This allows for quick changes to be uploaded into the processor, without having to remove the electronics from the field locations. The current functionality of the ColdFire is to collect data from the ADC for each channel, store the respective calibration data, as well as compute the positions based upon a Spline interpolation. Figure 3 shows an overall picture of the electronics with the on board processor in place.

FIGURE 3: BPM Electronics

Physical Requirements

A driving design requirement for these electronics was to have them within close proximity to the actual BPM can. This would eliminate the cost of the expensive cabling and connectors that previous systems have used. To accomplish this, these electronics were designed to fit underneath the magnet stands that are within the machine enclosure. These electronics still require communication, power, and timing signals, but this cabling is a fraction of the cost of running RF cables to instrumentation racks. The placement of the electronics within the magnet stand allows the case to be surrounded by steel and grout for excellent radiation and noise shielding. The picture showed in Fig. 4 shows how the electronics fit within the magnet girder.

FIGURE 4: BPM Electronics in the magnet girder

TESTING AND MEASUREMENTS

Calibration Data and Techniques

In order to compensate for variations of components and to get maximum resolution from these electronics a Spline interpolation of the RF input was implemented. This was done by injecting a RF input into the front end of each channel and using the ColdFire to record the data. In increments of 1 dBm, the RF input is varied from -50 dBm to 15 dBm. While data is being recorded, the ColdFire stores the response for each power input in a lookup table. Figure 4a shows typical calibration data for a set of electronics. The process programmed in the ColdFire uses this data to calculate beam position by using the equations in Fig. 4b [3].

FIGURE 4: Calibration Data for a set of electronics. Equation process for calculating position

Beam Measurements

The measurements made with the FEL beam were to look at the slope linearity of the BPM position readback as we varied the bunch frequencies of the FEL. This was done by setting the bunch frequency and then steering the beam ± 100 gauss in increments of 10 gauss in both the horizontal and vertical directions. This was done at different frequencies and then the responses were compared. The two graphs below in Fig. 5 show the linearity of the response as the beam is steered in both directions.

FIGURE 5: Linearity Response for different bunch frequencies. (a) Horizontal (b) Vertical

FUTURE PLANS AND DEVELOPMENTS

Currently there are six sets of these electronics installed in the FEL in various locations. Since this version was strictly done as a developmental version, several recommendations and future plans have been developed. One limitation to these prototype electronics is the throughput is limited to about 100 Hz. This limits the resolution that these electronics are capable of achieving. In order to improve the throughput to 1 MHz, the architecture of ADC to ColdFire will be changed to an architecture of ADC to FPGA to ColdFire. This will allow the FPGA to do fast data capture from the ADC while the ColdFire performs position calculations. With fast data capturing the capabilities of averaging and BPM parameter snapshots will both be available.

While testing these electronics it was found that the trigger timing is extremely important to the electronics functionality. The current method of triggering is an external "Beam Sync" signal that occurs with each macro pulse of the FEL beam. This signal requires the timing for each set of electronics to be time shifted based upon their location in the FEL. The proposed solution for this delay is to implement an internal trigger to accompany the external trigger. This internal trigger mode would use the RF Front End to trigger the sampling without the need of the external trigger. The internal triggering method would eliminate the need for one more cable therefore further reducing the cost of the electronics. Both methods are intended to be implemented with dual triggering options.

It is also intended for these electronics to utilize the Power over Ethernet (PoE IEEE802.3af) standard as to combine the power and communication cabling into one CAT-5 cable. Implementing PoE will make the electronics a stand alone device that requires only a PoE cable. This will set the cost for one set of BPM Electronics to approximately \$750.00 for all cabling, connectors, and electronics.

REFERENCES

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