Proposal for a Magnet Power Supply Interface and Control Chip Set*

N. J. Dobeck, J. Perry

Continuous Electron Beam Accelerator Facility
12000 Jefferson Avenue, Newport News, VA 23606 USA

Abstract

Significant advantages are obtainable if an interface and control chip set is developed which can be used with most magnet power supplies needed at accelerator facilities. This paper will show that such a chip set can be developed using currently available hardware and software technology. A proposed architecture will be presented and three common power supply applications discussed.

I. INTRODUCTION

The Accelerator Power Technologies group has been working to reach agreement on standardization of accelerator magnet power supply computer interfaces to reduce the cost of power supplies for the entire community. This paper proposes a small set of chips and/or modules that can be used in various combinations to cover a wide range of precision magnet power supply control and communications applications and demonstrates that hardware and software technology currently exist that very effectively complement interface standards presently under consideration. Consensus on interface standards and realization that powerful and inexpensive control hardware is within reach can lead to more capable and less expensive power supplies for users by providing a tighter focus for vendor product development.

Precision power supplies require the characteristic functions of high performance instrumentation and control systems. If we draw a block diagram of a high performance power supply (Fig. 1), we can define a set of standard interfaces, allowing us to design a small set of function modules which can be selected to implement a wide range of applications ranging from a simple, low cost corrector supply to a complex, high performance supply for synchrotron rings.

Fig. 1 Power Supply Functional Block Diagram

We give a brief description of the individual function blocks, then discuss three applications including a 100 ppm

bipolar corrector current regulator, a 10 ppm DC power supply and a unit suitable for use with a synchrotron ring. The first two applications will be emphasized since we have experience with these at CEBAF.

Communications Processor

This block communicates with the host control system under the standard power supply control protocol and interprets the system protocol for other modules. One communications processor may be allocated to one power supply or a subsystem of related power supplies. The modularity gained by standardizing this section would allow a vendor to comply with interface standards such as Intel's Bitbus with relatively little effort.

Interlock Processor

This block receives interlocks from all alarm and status sources associated with the individual power supply. One interlock processor may be allocated to one power supply or a subsystem of related power supplies. These signals are reformatted and transmitted to the host control system or may trigger local actions. Interlock programming may be done in ladder logic or any of several common languages.

Profile Processor

This block interprets the requested operating point of the power supply's output. It may be programmed to step to a specific point at a specific time, ramp from one point to another, or follow some function commanded by the communications processor. This is the first block in which an analog substitution may be made for the digital protocols, and which may have an analog output. It determines the accuracy of the supply's interpretation of input commands.

If the profile processor is implemented in software, its output must be a digital value corresponding to the requested current level. The servo processor accepts the profile processor's output as an input.

If the profile processor is implemented in analog hardware, the circuit's environment must be evaluated and possibly controlled to assure that the output conforms correctly to the desired value. This is not a problem with a software processor.

Where systems of supplies must be synchronized, an external clock may be implemented so that all subsystems coordinate their changes in current level.

Servo Processor

This block attempts to force the power supply output to the requested value by comparing the measured output with the output requested by the profile processor, and generating a control signal to correct any errors. This

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block, which may use either analog or digital techniques, or both, determines the long term (low frequency) stability and precision of the supply's response to input commands.

If the servo processor is implemented in analog hardware, the stability and gain of the analog section will determine the ultimate stability of the system's response to commands.

Power Converter

This block converts the control signal from the servo processor into regulated output current/voltage to the magnet(s). It gets its source power from the raw supply. It measures the output current and voltage and returns the measured values to the servo processor for comparison. The gain, ripple rejection and filtering of this block in conjunction with the load time constant determine the short term quality (high frequency response) of the output.

Raw Power Supply

The raw power supply changes the AC utility power to direct current at the current and voltage capacity specified for the magnet or magnet string to be driven. It should also do some preconditioning of the raw power, such as spike filtering and voltage preregulation, to improve the performance of the output. This block may also do power factor correction, which is becoming increasingly important as utilities and users become more conscious of AC power quality. One raw supply may be allocated to one power supply or a subsystem of related power supplies.

Auxiliary Processor

The optional auxiliary processor does sophisticated signal or parameter processing. One auxiliary processor may be allocated to one power supply or a subsystem of related power supplies.

The auxiliary processor would be used for complex on-line analysis of current or voltage disturbances, or it might aid the servo controller with extra processing power for advanced control algorithms incorporating feedforward control and disturbance compensation, or it could do data processing for maintenance analysis.

Alternatively, there might be a complete data acquisition system in the module for acquisition of data beyond those required for actual power supply control.

II. IMPLEMENTATION AS A CHIP SET

To spur serious consideration of the issue of standardization, and development of a compact controller package, we propose chip sets based on this organization, and indicate other possible dividing lines for chip sets.

Corrector Power Supply Emphasizing Separation of Analog and Digital Environments

Figure 2 is the block diagram of a typical bipolar corrector power supply. All the functions fit neatly into the conceptual block diagram described above, and all are useful if not essential to the needs of a modern accelerator magnet supply.

Fig. 2 Digitally Controlled Analog Based Power Supply

This design divides the conceptual diagram into three basic parts: analog functions, digital functions, and power functions. The embedded microcomputer handles only inherently digital functions, that is, the communications, interlock, and such auxiliary processing functions as a local terminal, internal diagnostics, and local data acquisition for performance monitoring.

There are a number of single chip microprocessors that would do this job quite well, and a well conceived standard for these digital functions, such as a common communications protocol and a high level interlock or discrete input/output language, would make it possible for the entire industry to specify a device based on this standard. Once the initial implementation is complete, the controller would be available to the entire accelerator industry, removing the need for new communicator/controller design work. This fact would make economical a far more complex controller than might be otherwise considered, since the cost of implementation would be spread over many more users. We note that interfaces that carefully consider user interface and performance optimization generally result in more complex software designs than interfaces that pay less attention to versatile interface requirements.

The portions of the conceptual model that are amenable to analog implementation are all implemented in analog circuitry in this example. The serial digital to analog converter and analog to digital converter implement the profile processor and the operational amplifier is the servo processor. If the component labeled Z is for example a capacitor, the servo is a proportional-integral type controller; if it is a resistor, the servo is a proportional only controller.

For this block, the analog circuitry may be implemented in high accuracy analog integrated circuitry and may be placed on a temperature stabilized block for improved stability. If standards are accepted in the accelerator community, this is another element that may be designed and implemented once and shared among many laboratories.

The bipolar output stage is the power converter, which again may be designed for a range of output capacities and shared among many laboratories. For this section we will need a standardized way to specify input and output signals and the conversion gain from the input drive signal to the output current level. A small set of voltage and current capacities will cover a wide range of uses.

Unfortunately, very high precision supplies will have very costly profile/servo blocks if they are implemented in fully analog form. The next example addresses this problem.

10 ppm DC Power Supply

The unipolar magnet supply illustrated in Figure 3 shows a system apparently similar to that of Figure 2, but note that there is no feedback amplifier in the servo controller.

Fig. 3 Digitally Operated Power Supply

This example uses software implemented profile generation and servo regulation to eliminate as much as possible the disadvantages of analog circuits. The only remaining analog functions are the precision reference, the digital-analog converter, and the analog-digital converter and DCCT burden resistor. Note that the DAC is buffered, and the response signal is amplified to force the driving and measured signals into the appropriate ranges of the conversion circuits.

The software of the profile generation will require a higher processor than the previous analog implementation; a digital signal processor as a primary control processor or attached auxiliary processor is an obvious candidate.

The tradeoff between this and the previous arrangement must be examined carefully for required speed of response and fidelity to demanded current level. Nevertheless, this arrangement offers the possibility of very high performance for very low cost.

Finally, synchrotrons require precisely coordinated

current ramps to stabilize the orbit of a beam accelerated in a restricted path. Figure 4 illustrates a method of accomplishing this end with external timing signals from a central controller. The timing signal may control a software process in a high performance processor or a separately implemented analog/digital block using only the digital controller from the first example for digital functions.

HIGH PERFORMANCE TRACKING POWER SUPPLY

Fig. 4 Synchronised Power Supply

III. SUMMARY

The technology now exists to design and build a small set of modules that can control any accelerator magnet power supply required. Making use of the similarity in control requirements over a broad range of magnet power supply applications, we have proposed to the Accelerator Power Technologies group a set of standard interfaces that will enable laboratories and vendors to cooperate in the design and construction of such a set of modules, which can allow us to devote more effort to solving difficult problems of general nature, then use these solutions repetitively among many laboratories. In this paper, we have proposed specific chip sets to implement this standard.

In this manner, we can build higher performance into our accelerators than would otherwise be economical, and avoid the substantial duplication of effort that exists now in the accelerator community.

IV. REFERENCES

- [1] Bork, R., Grubb, C., Lahti, G., Sage, J., "CEBAF Control System", 1988 Linear Accelerator Conference Proceedings.
- [2] Dobeck, N. J., Beaufait, J., Boettcher, E., Burtner, G., Francis, P., LaMora, R., O'Sullivan, M., Settles, C., Sharp, C., "Precision, 32 Channel Power Supply System", 1990 Linear Accelerator Conference Proceedings.