Superconducting Magnet Power Supply and Hard-Wired Quench Protection at Jefferson Lab for 12 GeV Upgrade

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Abstract—The superconducting magnet system in Hall B being designed and built as part of the Jefferson Lab 12 GeV upgrade requires powering two conduction cooled superconducting magnets—a torus and a solenoid. The torus magnet is designed to operate at 3770 A and the solenoid at 2416 A. Failure modes and effects analysis determined that voltage level thresholds and dump switch operation for magnet protection should be tested and analyzed before incorporating into the system. The designs of the quench protection and voltage tap subsystems were driven by the requirement to use a primary hard-wired quench detection subsystem together with a secondary programmable logic controller (PLC)-based protection. Parallel path voltage taps feed both the primary and the secondary quench protection subsystems. The PLC-based secondary protection is deployed as a backup for the hard-wired quench detection subsystem and also acts directly on the dump switch. We describe a series of tests and modifications carried out on the magnet power supply and the quench protection system to ensure that the superconducting magnet is protected against all fault scenarios.

Index Terms—Detection, dump switch, magnet, magnet protection, power supply, quench, superconductivity.

I. INTRODUCTION

HE torus magnet is one of the two conduction cooled superconducting magnets for 12 GeV upgrade project. This upgrade is for Experimental Hall B at Jefferson Lab (JLab) and forms part of the CEBAF Large Acceptance Spectrometer (CLAS12) [1], [2]. The magnet consists of six superconducting coils arranged to produce a toroidal magnetic field around the beam line (see Fig. 1). All six coils are electrically connected in series with joints of superconducting bus-bars. They are mounted directly onto the He circuit heat exchangers (recoolers) in order to conduction cool the splices. The overall inductance of the torus magnet is \sim 2.0 H with a stored energy of \sim 14 MJ at 3770 A [3]. The magnet is charged using a superconducting magnet power supply (MPS). This was a custom design

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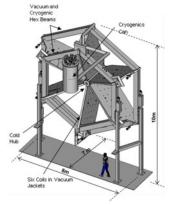




Fig. 1. CLAS12 torus magnet.

from Danfysik based on a model 8500/T854 [4]. The MPS dc output is low voltage, high current, designed for near zero resistance loads; however, the impedance seen at the magnet/power supply output terminals can go from pure inductive to an almost pure resistive state during a quench. Due to the requirements for high stability and low drift on a static magnetic field, a linear series-pass regulation topology was selected. The MPS circuit design allows variable sweep rates for ramping-up and -down the current in steps. The torus MPS output utilizes two quadrant operation allowing for smooth and continuous ramping of the current into the magnet. Magnetic field polarity reversal is achieved by means of a mechanical switch to reverse the direction of current flow (unlike a four-quadrant power supply). The power supply is programmed to sweep magnet currents at predetermined rates at different current levels without user intervention.

The power supply is designed to detect a quench and switches off power automatically. The hard-wired quench detection subsystem acts directly on the dump switch as a part of the primary protection system. The quench protection system is capable of detecting quench-induced voltages at multiple points namely magnet coils, bus-bars, and the whole magnet in the cryostat. The quench fault thresholds are set to the expected quench voltages derived from simulations. The voltage thresholds and the inductance of the magnet set upper limits on the MPS current ramp rate, in order to avoid false trips.

Magnet

Torus

Solenoid

 I_{OP}

(A)

 ± 3770

+2416

 L_{TOT}

(H)

2.0

6.0

Description	Specification		
Output current/voltage	±4000 A / ±6 VDC		
Ramp rate	Variable: ± 0.2 to ± 3.0 A/s		
Supply voltage	480 V/3-Φ/60 Hz.		
Ambient temperature	15–35 °C		
Cooling water (flow, temperature)	60 l/m, 15–35 °C		
Pressure	300 psig		
Ground Isolation	$> 1.0 \mathrm{M}\Omega$		
Quench protection	Fast de output breaker		

 E_{ST}

(MJ

14.21

17.50

 $R_{
m D\,UM\,P}$

 (Ω)

0.124

0.200

 $V_{\mathrm{D\,U\,M\,P}}$

< 500

< 500

 $T_{
m M\,A\,X}$

(°C)

< 350

< 350

TABLE I
TORUS-DC POWER SUPPLY AND FAST ENERGY DUMP SPECIFICATIONS

The magnet system was subjected to a failure mode and effects analysis (FMEA) process to evaluate the robustness of its protection system and adequacy of the instrumentation to monitor the performance of the magnet [5]. While the FMEA includes analysis of the magnet power system, cryogenics, instrumentation, mechanical stability, and many other factors, this discussion focuses solely on the MPS.

II. DC POWER SUPPLY—SUPERCONDUCTING MAGNET

The power supply employed on the torus and the solenoid magnet is a Danfysik Model 8500 rated at 4000 A/6 V, with an integrated dump resistor, 124 and 200 m Ω for the torus and the solenoid, respectively [4]. The MPS incorporates features designed to mitigate or prevent failure modes during the magnet operation. These features include: controlled current ramping (up or down), fast dump switch and resistor to de-energize the magnet, integrated polarity reversal switch, slow dump capability, and multiple dc current transducers for current-based interlocks. Additionally, a separate rack mounted programmable logic controller (PLC)-based controller initiates/programs ramp rate of the current, monitor's interlocks on the magnet, and checks the overall health of the magnet. Salient MPS and energy dump specifications are given in Table I.

III. SUPERCONDUCTING MPS TEST

As part of the magnet energization process and readiness review, hi-pot, interlock functionality, full output current test with shorted terminals, and evaluation of the test dump switch opening times were established toward system realization.

A hi-pot test, (with measurement of the leakage current) was successfully completed at 1 kV. To perform the hi-pot test, ground fault leakage current resistor was temporarily removed. Interlock functionality was also successfully tested and verified. Subsequently, a full output current test at 4000 A was successfully performed upon shorting the terminals after the water-cooled leads.

The power supplies employed for the torus and the solenoid were adequate by design having a total time delay of <750 ms between quench set threshold is exceeded and the time for the dump switch to fully open during energizing and operation for

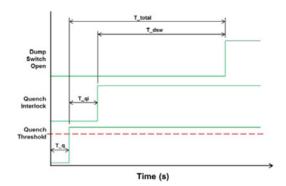


Fig. 2. Representation of timing diagram for quench detection.

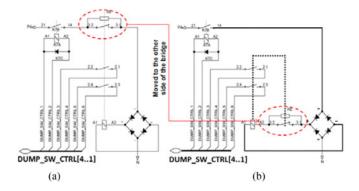


Fig. 3. Dump switch coil configuration: (a) Danfysik factory setting and (b) with JLab modification.

magnet safety. With similar power supplies across the laboratory, the suggestion was to improve on the overall delay using the mechanical breaker. Danfysik system consists of an integrated mechanical breaker along with quench detector (QD). Any improvement on the overall delay helps us to keep the hot spot temperature in the superconductor low (<150 K) during a quench event. Switching the power supply off during any magnet quench condition is crucial for the safety of the superconducting magnet and the MPS. The timing diagram for the quench detection process is shown in Fig. 2. The time is divided into three parts.

- 1) T_q (s) is the time between quench initiation and quench threshold is exceeded,
- 2) T_qi (s) is the time between when the quench threshold is exceeded and the quench-interlock relay contact opening, which is a constant attributed to the associated electronics (see Fig. 3),
- 3) T_dsw (s) is the subsequent time for the dump switch to fully open. As shown in Fig. 4, T_qi is measured to be about 12 ms, T_dsw is measured to be about 580 ms, and T_total is about 600 ms.

A complete quench detection timing analysis and the modifications of the dump switch timing circuit have been carried out at JLab. The initial tests carried out on the MPS with the factory setting for the timing of the opening of the dump switch measured $\sim\!600$ ms, shown in Fig. 5, based on the factory configuration shown in Fig. 3(a). After conferring with the MPS and the dump switch manufacturers, the dump switch circuitry was reconfigured as shown in Fig. 3(b). The reconfiguration involved changing the series-connected dump switch coil resistor

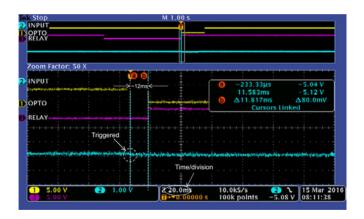


Fig. 4. Traces showing quench interlock detection timing.

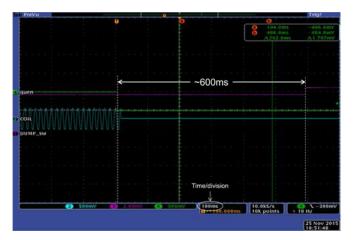


Fig. 5. Traces showing the dump switch timing with factory setting from vendor is about 600 ms to open.

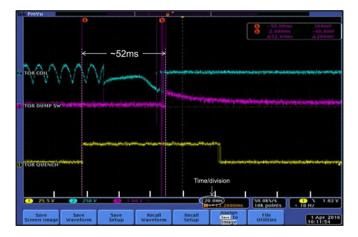


Fig. 6. Traces showing the dump switch timing after JLab modification is about 60 ms to open.

to be in parallel with the dump switch coil. The value of the resistor, RE, was also increased from 1.0 to 1.25 k Ω in order to decrease the switching time. The modification significantly reduced the T_total time to \sim 60 ms as shown in Fig. 6. The overall time from quench initiation to dump switch opening is estimated to be less than 120 ms (T_qi = 30 ms and T_dsw = 90 ms) which is significantly lower than the 600 ms measured prior to the modifications [6].

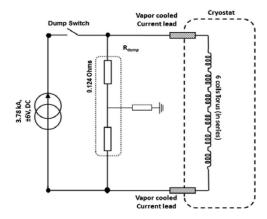


Fig. 7. Schematic arrangement of torus magnet dump resistor in protection circuit

IV. QD BOARD CONFIGURATION

The design of the quench protection (see Fig. 7) and voltage tap subsystems were driven by the anticipated level of voltages developed during a magnet quench and a full FMEA process [7]–[9]. A dual protection scheme is employed, where a primary hard-wired analog circuit works in conjunction with a digital PLC-based circuit. Parallel paths feed the primary and secondary quench protection subsystems. The primary hardwired quench detection system was provided as standard by Danfysik. Each quench detection module consists of four differential input channels. Each input channel is capable of local balancing and varying/adjusting the delay that acts directly to convey a relay contact state for the MPS to open the fast dump switch. The secondary quench detection is performed in the PLC, where voltage tap data is fed from a second dedicated unit with eight four-channel N9239 24-bit analog input modules. The digitized voltages are compared against user-selected thresholds, in software, to turn the MPS OFF and activate the fast dump switch, when a fault condition is detected.

Integrated QD units are capable of detecting the fault conditions that may arise both in the superconducting magnet coils or in the vapor-cooled current leads at least across two channels. The magnet diagnostic system (MDS) is associated with the control and the data acquisition (DAQ) subsystems. The MDS has been engineered to include a hard-wired interlock safety system. It will protect each magnet system in the event any selected magnet parameter or limit exceeds user-set thresholds. The MDS primarily monitors voltages across the coils, magnet water-cooled bus-bars, splices, and the vapor-cooled current leads.

The quench protection system, mechanical dump switch, interlocks, and remote control systems were all tested and verified for reliable operation/functioning as expected during normal steady-state magnet operation at 3770 A. During the commissioning of the MPS, maximum current applied across the shorted terminals was 4 kA in the forward and the reverse directions. Gains across the channels of the QD's (end of comparator) were carefully tuned and set to hard-wired detection threshold voltages. The threshold voltages are based on the results of quench analysis under various conditions. The differential output

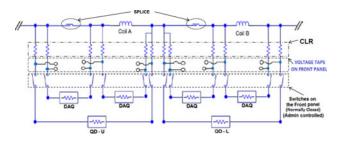


Fig. 8. Circuit used for impedance-matching simulations—CLR, Op-Amp, and QD board.

voltages across the QD channels (output of the amplifier into the comparator) are adjustable over the range of 2 mV to 2.0 V under fault condition. The quench detection unit triggers the energy dump circuit, when a fast magnet current ramp-down is sensed via a direct analog interlock, once the differential set threshold is reached.

For risk assessment and mitigation (RAM) planning, rigorous and repetitive tests were carried out with an artificial quench signal (differential voltage) sent to the quench protection system. Both primary and the secondary quench protection system tests were completed satisfactorily for reliability and repeatability. The MPS has compatibility using RS 232/422/485 remote control access with in-built safety features, e.g., ramping-down the current automatically in the event of a power loss, a temperature rise, an open interlock, etc.

One of the design features in the QDs of the torus magnet was to have a patch panel for routing the voltage signals and to allow for local diagnostics. The voltage taps, mentioned earlier, are wired into the input terminals on the patch panel. These current-limited signals are then routed to the QD or the DAQ circuitry, sometimes in parallel. DAQ consists of isolated amplifier feeding the input of National Instruments ADC module, sampled using N.I.'s CompactRIO (cRIO). Further, cRIO transmits the sampled data to a PLC which then is used for decision making. The voltage tap signals meet national fire protection association (NFPA) 70E Class-I limits with the addition of current-limiting resistors (CLRs). These CLRs, in turn, affect the input impedance of the factory configured QD circuits and their associated DAQ channels. The modifications were carried out on the standard off-the-shelf QD boards from Danfysik in order not to exceed predetermined circuit-loading requirements. With QD and DAQ systems in parallel, the result in a complex voltage divider network that needed the modifications as carried out to balance the circuit/s. To modify the QD boards to comply with Class-I requirements, it was necessary to overcome the balancing issue across the voltage taps in QD's that share a common node with DAQ's in parallel as shown in Fig. 8. The DAQ impedance, primarily from the op-amp with 380 k Ω and QD impedance, $\sim 15 \text{ k}\Omega$, has two 150 k Ω CLRs connected in series. This suggests that the total impedance seen across the DAQ only is of the order of \sim 680 k Ω in comparison to the total impedance across the QD's only which is $\sim 315 \text{ k}\Omega$. Therefore, the imbalances with the DAQ included produce significant dips in the measured voltages across the magnet due to the impedance mismatch. QD simulation results along with the measured values are shown in Fig. 9.

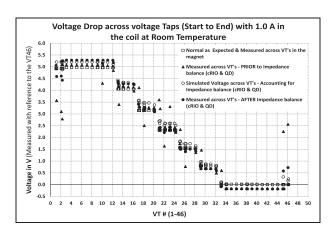


Fig. 9. Voltage across QD's and voltage taps across torus magnet—simulated and measured with adopted impedance matching modifications.

 $\label{thm:torus} \begin{tabular}{ll} TABLE \ II \\ TORUS \ QD \ RESISTOR \ VALUES—BEFORE \ AND \ AFTER \ IMPEDANCE \ MATCHING \\ \end{tabular}$

CLR (kΩ)		QD Impedance $(k\Omega)$		Potentiometer resistance $(k\Omega)$		Dividing Resistors on the QD board $(k\Omega)$	
X	Y	X	Y	X	Y	X	Y
150	50	14.75	300	0.1	2.0	2.0	49.9

X: Before modifications carried out.

In order to mitigate the impedance mismatch, a number of simulations using LTSpice were carried out with varying CLRs and resistors on the QD board (modular design in order to keep consistent across channels and spares) [10]. These simulations capture all QD and DAQ setup presets across all channels envisaged for the torus magnet protection system. The balancing potentiometer and divider are modified in order to obtain the same linearity of input voltage. The optimized solution is shown in Table II, complying with all Class-I requirements.

After carrying out the modifications on the input resistors (based on the simulations), measured and simulated values agree. The worst case observed before modifications is at the start and end of the magnet leads. It is measured $\sim\!2.75$ V compared to $\sim\!4.4$ V after modification, against 5.0 V as simulated. The ΔV of 600 mV can be attributed to three DAQ channels connected to a single node compared to one DAQ channel.

V. BENCH SETUP AND TESTS

As part of a RAM program at JLab, the modified QD boards were tested on the bench with a voltage-divider circuit and a potentiometer for adjusting the balance, as shown in Fig. 10, before incorporation into the protection system. This adjustable voltage divider circuit mimics quench threshold voltages from 100 mV to 2.25 V. In the bench setup, output of the adjustable voltage-divider circuit was connected to 50 k Ω series resistors going to the upper and the lower input sections of the quench voltage detection channel. The tests confirmed that 50 k Ω series resistors were indeed suitable to allow setting of the gains on the QD boards.

Y: Optimized values after carrying out simulations and adopted in the final configuration.

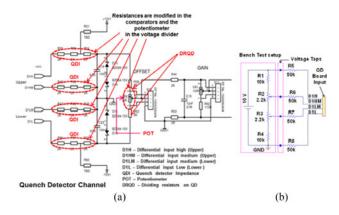


Fig. 10. (a) Schematic layout generic QD board circuit diagram provided by Danfysik and modifications carried out on the boards. (b) Schematic layout of the test set up after modifications on the board.

VI. SUMMARY

Both power supplies for superconducting magnets in Hall B at JLab were commissioned in May 2016. Both power supplies are modified to: 1) accommodate the impedance matching of CLR with QD and DAQ input impedance, 2) decrease overall fast dump switching time after a quench event to <120 ms. Successful multiple fast dumps up to 3.0 kA were carried out with the integrated MPS on the torus during the magnet system commissioning phase, with triggering via both primary and the secondary protection subsystems. The torus MPS and magnet are successfully integrated and are fully operational in Hall B.

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REFERENCES

- [1] C. Rode, "Jefferson lab 12 GeV upgrade," in *Proc. Adv. Cryo. Eng. Conf.*, 2010, vol. 1218, pp. 26–33.
- [2] R. J. Fair and G. L. Young, "Superconducting magnets for the 12 GeV upgrade at Jefferson laboratory," *IEEE Trans. Appl. Supercond.*, vol. 25, no. 3, Jun. 2015, Art. no. 4500205. doi: 10.1109/TASC. 2014.2365737.
- [3] P. K. Ghoshal et al., "Electromagnetic and mechanical analysis of the coil structure for the clas12 torus for 12 GeV upgrade," *IEEE Trans.* Appl. Supercond., vol. 25, no. 3, Jun. 2015, Art. no. 4500705. doi: 10.1109/TASC.2014.2382604.
- [4] C. Neilsen, "Design report USA 502337-201, Hall B, torus/solenoid MPS," Danfysik, Taastrup, Denmark, MPS 854 - Danfysik Syste. 8500, Jun. 2014. [Online]. Available: www.danfysik.com.
- [5] P. K. Ghoshal et al., "FMEA on the superconducting torus for the jefferson Lab 12 GeV accelerator upgrade," *IEEE Trans. Appl. Supercond.*, vol. 25, no. 3, Jun. 2015, Art. no. 4901005. doi: 10.1109/TASC.2015.2388591.
- [6] S. Philip, "JLab Hall-B torus power supply setup and acceptance testing," Jefferson Lab Anal., Newport News, VA, USA, Rep. B000000401-R017, Apr. 2016.
- [7] P. K. Ghoshal and R. Rajput-Ghoshal, "Quench analysis-single coil quench analysis using Wilson model (analytical)," Jefferson Lab Anal., Newport News, VA, USA, Rep. B000000401-A012, Apr. 2013.

- [8] V. Kashikhin et al., "Torus CLAS12-superconducting magnet quench analysis," *IEEE Trans. Appl. Supercond.*, vol. 24, no. 3, Jun. 2014, Art. no. 4500405. doi: 10.1109/TASC.2014.2299531.
- [9] P. K. Ghoshal, G. Biallas, R. J. Fair, C. Luongo, and R. Rajput-Ghoshal, "Design of quench tolerant sections in coil leads and splices for torus magnet at jefferson lab," Jefferson Lab Anal., Newport News, VA, USA, Rep. B000000401-A027, May 2016.
- [10] Linear Technology, Milpitas, CA, USA, "Open source design tool for electrical engineers, 'LTspice'." 2016. [Online]. Available: http://www.linear.com/designtools/software/

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